IN THE CLAIMS

1. (Currently Amended) A signal processor for processing a predetermined unit of input data containing a variable length code and information providing the active length of the variable length code, said signal processor comprising:

input means for inputting the input data;

start detecting means for detecting the start of the predetermined unit of the input data, in which the predetermined unit corresponds to a frame;

means for receiving a frame end signal indicative of the end of a number of frames;
end detecting means for detecting the end of a respective frame based on the frame end
signal the predetermined unit of the input data input by said input means based on the
information providing the active length; and

signal processing means for making an action on the variable length code active at the start detected by said start detecting means, for making the action on the variable length code inactive at the end detected by said end detecting means, and for initializing the state of the action on the variable length code at the end detected by said end detecting means.

- 2. (Original) A signal processor according to Claim 1, wherein the input data comprises MPEG encoded data.
- 3. (Original) A signal processor according to Claim 1, further comprising recording means for recording the output of said signal processing means.

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4. (Currently Amended) A signal processing method for processing a predetermined unit of input data containing a variable length code and information providing the active length of the variable length code, said signal processing method comprising the steps of:

inputting the input data;

detecting the start of the predetermined unit of the input data input in said inputting step, in which the predetermined unit corresponds to a frame;

receiving a frame end signal indicative of the end of a number of frames;

detecting the end of a respective frame based on the frame end signal the predetermined unit of the input data input in said inputting step based on the information providing the active length; and

performing processes to make an action on the variable length code active at the start detected in said start detecting step, to make the action on the variable length code inactive at the end detected in said end detecting step, and to initialize the state of the action on the variable length code at the end detected in said end detecting step.

- 5. (Original) A signal processing method according to Claim 4, further comprising the step of recording the result of said process performing step.
- 6. (New) The signal processor according to claim 1, wherein the means for receiving includes a flip-flop circuit.

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7. (New) A method for processing frames of data comprising:

synchronizing a frame end signal with end of frame data that indicates an end of each frame;

processing each frame until the end of frame data is detected;
suspending processing for a period of time, the period of time being from the end of
frame data to a subsequent start signal, when an error is detected;

detecting a start code for a corrected stream of data; and re-initiating the processing step as a function of the detecting step.

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